

Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) Reconfigurable signal processing architecture

including comprising a reconfigurable data processing module in which data is input to the module in a packet frame structure including configuration frames and processing frames, each frame including a header having at least one mode selection bit indicating whether the frame contains reconfiguration data or processing data, and in whichwherein the module is operable in a reconfiguration mode or a processing mode according to the contentresponsive to of the frame header and the mode selection bits are separated from the data in each frame and are used to control mode selection logic in the module for determining how incoming data is handled.

2. (Currently Amended) Architecture as claimed in claim 1 including

comprising a plurality of reconfigurable data processing modules each of which receives data in said packet frame structure and each of which is operable in a reconfiguration mode or a processing mode according to the content of the frame header.

3. (Original) Architecture as claimed in claim 2 in which the frame header

contains at least one mode selection bit for each of the modules.

4. (Original) Architecture as claimed in claim 3 in which the mode selection bits

are decoded by a single decoder serving a plurality of modules.

5. (Original) Architecture as claimed in claim 4 in which the decoded mode

selection data is supplied to the modules in parallel.

6. (Original) Architecture as claimed in ~~any of claims claim 2 to 5~~ in which the modules are connected to each other in series.

7. (Currently Amended) Architecture as claimed in ~~any preceding claim 1~~ in which ~~the or each module at least one of the modules~~ is additionally operable in a bypass mode in which incoming data is not acted on by the module and in which the header additionally indicates whether or not the module is to act on the data.

8. (Currently Amended) A radio ~~transmitter and/or receiver~~ signal processing apparatus in which signals are processed digitally ~~after reception/before transmission~~, in which at least some components of the digital processing section of the ~~transmitter/receiver~~ apparatus are configurable and incorporate architecture as claimed in ~~any preceding claim 1~~.

9. (Currently Amended) Architecture as claimed in ~~any preceding claim 1~~ in which default/start up configuration data is supplied to the ~~at least one~~ module(s) from memory outside the ~~at least one~~ module(s).

10. (New) A radio signal processing apparatus according to claim 8 wherein the apparatus is selected from a group consisting of a receiver, a transmitter or a transceiver.

11. (New) Architecture as claimed in claim 1 including a plurality of said reconfigurable data processing modules wherein each of the modules is configured to be operated in a bypass mode in which incoming data is not acted on by the module and in which the frame header additionally indicates whether or not the module is to act on the data.